2.9 GHz PLL for SAT TV Receiver with Universal Bus

Description

The U6223B is a single-chip PLL for SAT-TV tuners. It contains all functions required for PLL control of a VCO. This IC also contains a high frequency prescaler and can handle frequencies up to 2.9 GHz.

The U6223B has a programmable 256/512/1024 reference divider, while the U6225B has a fixed reference divider of 512.

Features

- 2.9 GHz divide-by-16 prescaler integrated
- 3 selectable reference divider ratios:
  ÷256 / ÷512 / ÷1024
- Universal bus:
  I²C bus **or** 3-wire bus
  I²C bus software compatible to U6204B
  3-wire bus software compatible to U6358B (19 bit)
- I²C bus mode:
  5 switching outputs (open collector)
  4 addresses selectable at Pin 10 for multituner application
- 3-wire bus mode:
  4 switching outputs (open collector)
  Lock-signal output (open collector)
- Low power consumption (typical 5 V / 23 mA)
- Electrostatic protection according to MIL-STD 883

Benefits

- Only one device for 3-wire bus applications and I²C bus applications necessary (universal bus)
- High input frequency of 2.9 GHz applicable for all TV satellites

Ordering Information

Extended Type Number	Package	Remarks
U6223B-FP	SO16	Taped and reeled

Block Diagram

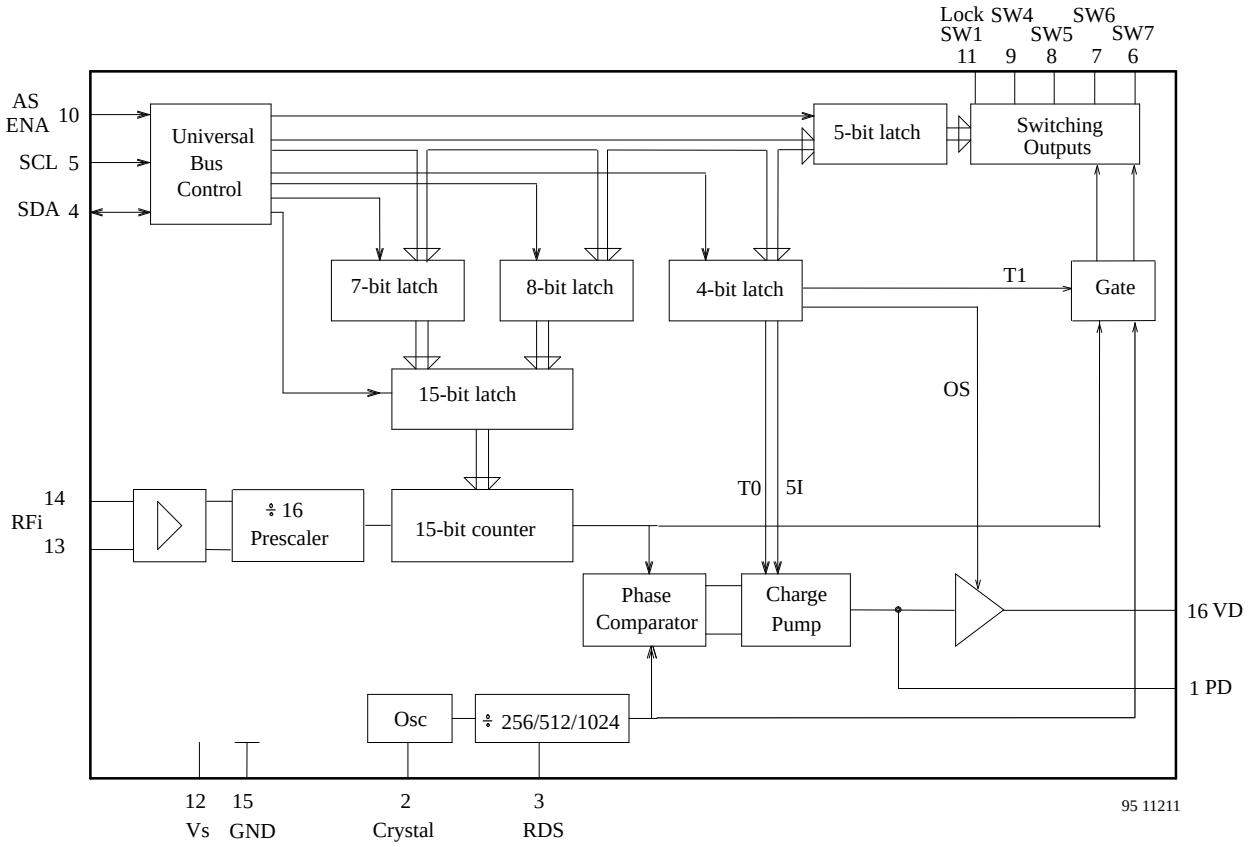


Figure 1. Block diagram

Pin Description

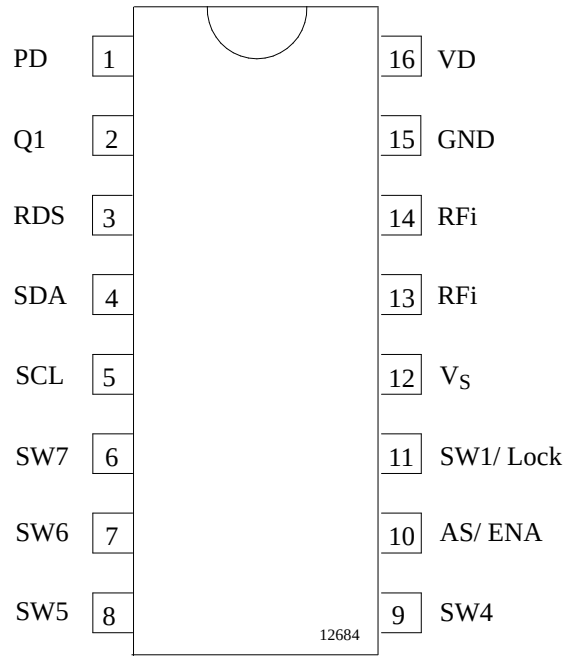


Figure 2. Pinning

Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	Crystal
3	RDS	Reference divider switch
4	SDA	Data in/output
5	SCL	Clock input
6	SW7	Switching output (open collector)
7	SW6	Switching output (open collector)
8	SW5	Switching output (open collector)
9	SW4	Switching output (open collector)
10	AS / ENA	Address select / enable input
11	SW1 / Lock	Switching / lock output (open collector)
12	Vs	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15)

Parameters		Symbol	Value	Unit
Supply voltage	Pin 12	Vs	–0.3 to 6	V
RF input voltage	Pin 13, 14	RFi	–0.3 to Vs +0.3	V
Switching output current open collectors	Pin 6–9, 11	SW 1, 4–7	–1 to 15	mA
Total current of switching outputs open collectors	Pin 6–9, 11	SW 1, 4–7	50	mA
Switching output voltage	Pin 6–9, 11	SW 1, 4–7		
in OFF state:			–0.3 to 14	V
in ON state:			–0.3 to 6	V
Bus input/output voltage	Pin 4	VSDA	–0.3 to 6	V
	Pin 5	VSCL	–0.3 to 6	V
SDA output current open collector	Pin 4	ISDA	–1 to 5	mA
Address select voltage	Pin 10	VAS / ENA	–0.3 to V_S +0.3	V
Charge pump output voltage	Pin 1	PD	–0.3 to V_S +0.3	V
Active filter output voltage	Pin 16	VD	–0.3 to V_S +0.3	V
Crystal oscillator voltage	Pin 2	Q1	–0.3 to V_S +0.3	V
Reference divider switch voltage,	Pin 3	RDS	–0.3 to V_S +0.3	V
Junction temperature		T_j	–40 to 125	°C
Storage temperature		T_{stg}	–40 to 125	°C

Operating Range

All voltages are referred to GND (Pin 15)

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	Vs	4.5		5.5	V
Ambient temperature		T_{amb}	–20		+85	°C
Input frequency	Pin 13, 14	R_{Fi}	250		2900	MHz
Programmable divider		S_F	256		32767	

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	110	K/W

Electrical Characteristics

Test conditions: V_S = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	SW 1, 4, 5, 6, 7 = 0 Pin 12	Is	18	23	28	mA
Input sensitivity						
Input frequency	fi = 250 MHz, Pin 13 fi = 750-2900 MHz, Pin 13	Vi [1] Vi [1]	100 20		300 300	mVrms mVrms
Crystal oscillator						
Recommended crystal series resistance			10		200	Ω
Crystal oscillator drive level	Pin 2			50		mVrms
Crystal oscillator source impedance	Nominal spread ±15% Pin 2			–650		Ω
External reference input frequency	AC coupled sinewave Pin 2		2		8	MHz
External reference input amplitude	AC coupled sinewave Pin 2		70		200	mVrms
Switching outputs (SW4–7, 1/ lock Pin 6–9, 11), lock output, (open collector)						
Leakage current	VH = 13.5 V	IL			10	µA
Saturation voltage	IL = 10 mA	VSL [2]			0.5	V
Charge pump output (PD)						
Charge pump current ‘H’	5I = H, VPD = 2 V Pin 1	IPDH		±180		µA
Charge pump current ‘L’	5I = L, VPD = 2 V Pin 1	IPDL		±50		µA
Charge pump leakage current	T0 = 0, VPD = 2 V Pin 1	IPDTRI		±5		nA
Charge pump amplifier gain	Pin 1, 16			6400		
Bus inputs (SDA, SCL)						
Input voltage	Pin 4, 5 Pin 4, 5	Vi ‘H’ Vi ‘L’	3		5.5 1.5	V V

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Input current	VSCL 'H' = V_S VSCL 'L' = 0 V	Pin 4, 5 Pin 4, 5	li 'H' li 'L'	 –10		10	µA µA
Leakage current	V_S = 0 V	Pin 4, 5	IL			10	µA
Output voltage SDA (open collector)	ISDA 'L' = 2 mA,	Pin 4	VSDA 'L'			0.4	V
Address selection / Enable input (SA, ENA)							
Input current	VAS 'H' = Vs VAS 'L' = 0	Pin 10 Pin 10	liAS 'H' liAS 'L'	 –100		10	µA µA

1) RMS-voltage calculated from the measured available power on 50 Ω
2) Tested with one switch active, the collector voltage may not exceed 6 V

Description

The U6223B is a single chip PLL designed for SAT receiver systems. It consists of a divide-by-16 prescaler (up to 2.9 GHz) with an integrated preamplifier, a 15-bit programmable divider, a crystal oscillator with a reference divider with three selectable divider ratios (÷256 / ÷512 / ÷1024), and a phase/ frequency detector together with a charge-pump, which drives the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via a I^2C bus format or the 3-wire bus format. It detects automatically which bus format has been received. Therefore, there is no need for a bus selection pin. In I^2C bus mode the device has four programmable addresses, programmed by applying a specific input voltage to the address select input, enabling the use of up to four synthesizers in a system. The same pin serves in 3-wire bus mode as the enable signal input. Five open collector outputs for switching functions are included which are capable of sinking at least 10 mA. One of these open collector outputs serves as a locksignal output in the 3-wire bus mode.

Functional Description

The U6223B is programmed via a 2-wire I^2C bus or 3-wire bus depending on the received data format. The three bus inputs pins 4, 5 and 10 are used as SDA, SCL and address select inputs in I^2C bus mode and as data, clock and enable inputs in 3-wire bus mode. The data includes the scaling factor SF (15-bit) and switching output information. In I^2C-bus mode, there are some additional functions for testing of the device included.

Oscillator Frequency Calculation

fvco = 16 * SPF * frefosc / SRF

fvco: Locked frequency of voltage-controlled oscillator
SPF: Scaling factor of programmable 15-bit divider
SRF: Scaling factor of reference divider: ÷256 / ÷512 / ÷1024
frefosc: Reference oscillator frequency: 3.2 / 4 MHz crystal or external reference frequency

The input amplifier together with a divide-by-16 prescaler provides excellent sensitivity (see 'Typical Prescaler Input Sensitivity'). The input impedance is shown in the diagram 'Typical Input Impedance'. When a new divider ratio according to the requested fvco is entered, the phase detector and charge pump together with the tuning amplifier adjusts the control voltage of the VCO until the output signals of the programmable divider and the reference divider are locked and phase locked. The reference frequency may be provided by an external source capacitively coupled into Pin 2, or by using an on-board crystal with an 18 pF capacitor in series. The crystal operates in the series resonance mode. The reference divider division ratio is selectable to ÷256 / ÷512 / ÷1024. Therefore, with a 4 MHz crystal and nominal division ratio of 512 of the reference divider the comparison frequency is 7.8125 kHz, which gives 125 kHz steps for the VCO, or with a 3.2 MHz crystal respectively 6.25 kHz comparison frequency and 100 kHz VCO step size. In addition, there are switching outputs available for bandswitching and other purposes.

Application

The U6223B is function and pin equiralent to the U6225B apart from the switchable reference divider. A typical application is shown on page 12. All input/ output interface circuits are shown on page 9. Some special features which are related to test- and alignment procedures for tuner production, are explained together within the following bus mode description.

I²C-Bus Description

When the U6223B is controlled via a 2-wire I²C bus format, then data and clock signals are fed into the SDA and SCL lines respectively. The table 'I²C-BUS DATA FORMAT' describes the format of the data and shows how to select the device address by applying a voltage at Pin 10. When the correct address byte has been received, the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. The table 'I²C BUS PULSE DIAGRAM' shows some possible data transfer examples.

Programmable divider bytes PDB1 and PDB2 are stored in a 15-bit latch and control the division ratio of the 15-bit programmable divider. The control byte CB1 enables the control of the following special functions:

- 5I-bit switches between low and high-charge pump current
- T1-bit enables divider test mode when it is set to logic 1
- T0-bit enables the charge pump to be disabled when it is set to logic 1
- RD1 and RD2-bit allow to select the reference divider factor
- OS-bit disable the charge pump drive amplifier output when it is set to logic 1.

The charge pump current can only be controlled in I²C bus mode. In 3-wire bus mode, there is always the high charge pump current active. The OS-bit function disables the complete PLL function. This enables the tuner alignment by supplying the tuning voltage directly through the 30 V supply voltage of the tuner.

The control byte CB2 programs the switching outputs SW 1, 4, 5, 6, 7; a logic 0 for high impedance output (off) and a logic 1 for low impedance output (on).

Description	I²C-Bus Data Format								
	MSB								LSB
Address byte	1	1	0	0	0	AS1	AS2	0	A
Programmable divider, byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Programmable divider, byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	X	RD2	RD1	OS	A
Control byte 2	SW7	SW6	SW5	SW4	X	X	SW1	X	A

A = Acknowledge; X = not used; Unused bits of controlbyte 2 should be 0 for lowest power consumption

n0 ... n14	Scaling factor (SF)	SF = 16384xn14+8192xn13+ ... +2xn1 + n0
T0, T1	Testmode selection	T1 = 1: divider test mode on T1 = 0: divider test mode off T0 = 1: charge pump disable T0 = 0: charge pump enable
SW1, 4, 5, 6, 7	Switching outputs	SW1, SW4, SW5, SW6, SW7 = 1: open collector active
5I	Charge pump current switch	5I = 1: high current 5I = 0: low current
OS	Output switch	OS = 1: varicap driver disable OS = 0: varicap drive enable
RD1, RD2	Reference divider selection	
AS1, AS2,	Address selection Pin 10	

RD2	RD1	Reference Divider Ratio
0	0	1024
0	1	off
1	0	256
1	1	512

AS1	AS2	Address	Dec. Value	Voltage at Pin 10
0	1	1	194	open
0	0	2	192	0 to 10% V_S
1	0	3	196	40 to 60% V_S
1	1	4	198	90 to 100% V_S

I²C-Bus Description (continued)

I²C-Bus Pulse Diagram

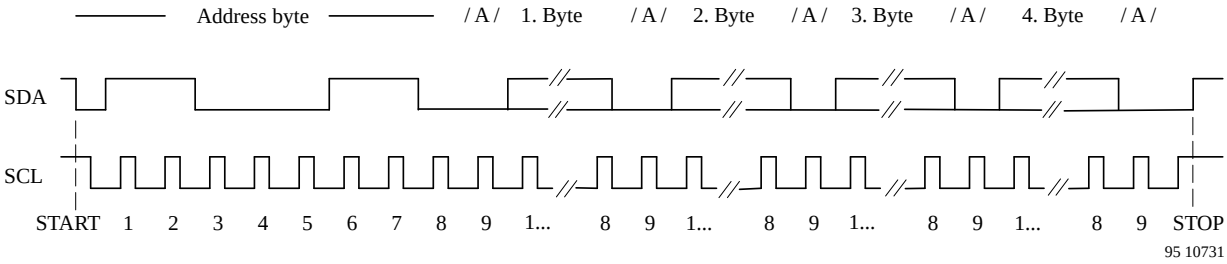


Figure 3.

Data transfer examples
START ADR PDB1 PDB2 CB1 CB2 STOP
START ADR CB1 CB2 PDB1 PDB2 STOP
START ADR PDB1 PDB2 CB1 STOP
START ADR CB1 CB2 PDB1 STOP
START ADR PDB1 PDB2 STOP
START ADR CB1 CB2 STOP
START ADR CB1 STOP

Description
START = Start condition
ADR = Address byte
PDB1 = Programmable divider, byte 1
PDB2 = Programmable divider, byte 2
CB1 = Control byte 1
CB2 = Control byte 2
STOP = Stop condition

I²C Bus Timing

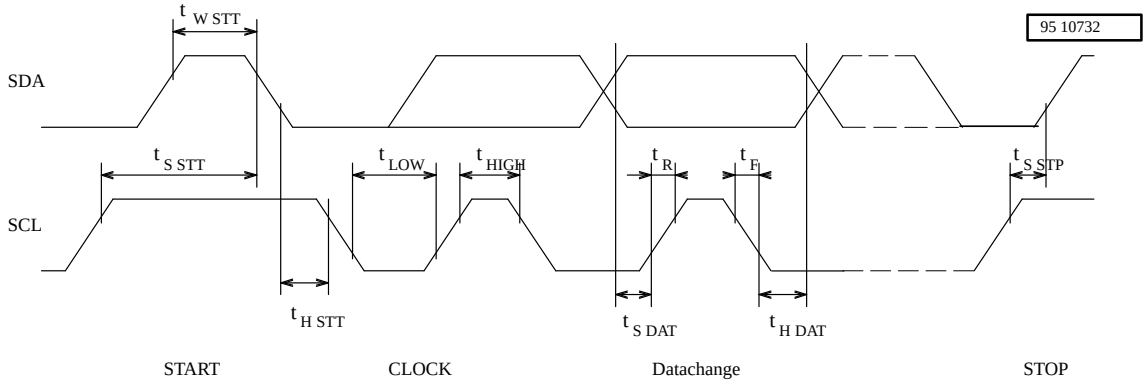


Figure 4.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Rise time SDA, SCL	tR			15	µs
Fall time SDA, SCL	tF			15	µs
Clock frequency SCL	fSCL	0		100	kHz
Clock ‘H’ pulse	tHIGH	4			µs
Clock ‘L’ pulse	tLOW	4			µs
Hold time start	tH STT	4			µs
Waiting time start	tW STT	4			µs
Set-up time start	tS STT	4			µs
Set-up time stop	tS STP	4			µs
Set-up time data	tS DAT	0.3			µs
Hold time data	tH DAT	0			µs

3-Wire Bus Description

When the U6225B-B is controlled via 3-wire bus format, then DATA, CLOCK and ENABLE signals are fed into the SDA, SCL and AS/ENA lines respectively. The diagram '3-WIRE-BUS PULSE DIAGRAM' shows the data format. The data consist of a single word, which contains the programmable divider and switch information. The data is only clocked into the internal data shift register on the negative clock transition during the enable lung period on the negative clock transition. During enable low periods, the clock input is disabled. New data words are only accepted by the internal data latches from the shift register on a negative transition of the enable signal if exactly nineteen clock pulses were sent during the high period. The data sequence and the timing is described in the following diagrams.

In 3-wire bus mode Pin 11 automatically becomes the lock-signal output. An improved lock detect circuit generates a flag when the loop has attained lock. 'In lock' is indicated by a low impedance state (on) of the open collector output.

In 3-wire bus mode, the high charge-pump current active. Only in I^2C bus mode can the charge-pump current is always be controlled.

The complete PLL function can be disabled by programming a division ratio of zero which is not normally used. This enables the tuner alignment by supplying the tuning voltage directly through the 30 V supply voltage of the tuner.

3-Wire Bus Pulse Diagram

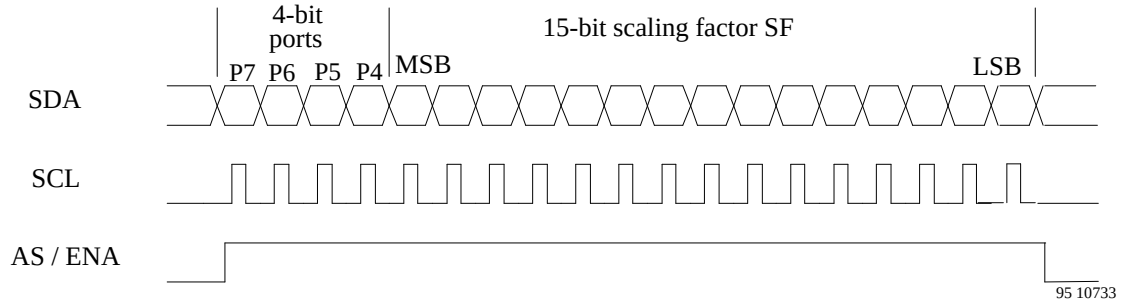


Figure 5.

3-Wire Bus Timing

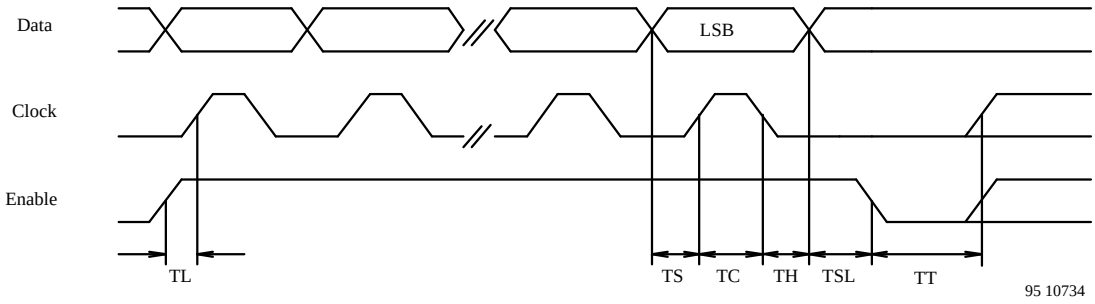


Figure 6.

Parameters	Symbol	Min.	Typ.	Unit
Set up time	TS	2		µs
Enable hold time	TSL	2		µs
Clock width	TC	2		µs
Enable set up time	TL	10		µs
Enable between two transmissions	TT	10		µs
Data hold time	TH	2		µs

Input/Output Interface Circuits

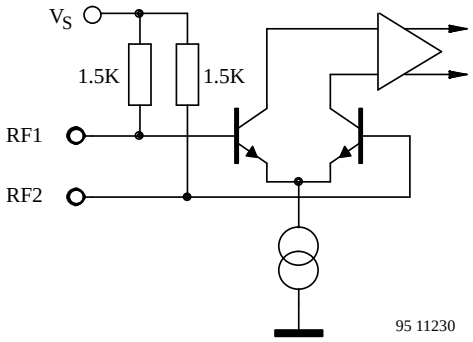


Figure 7. RF input

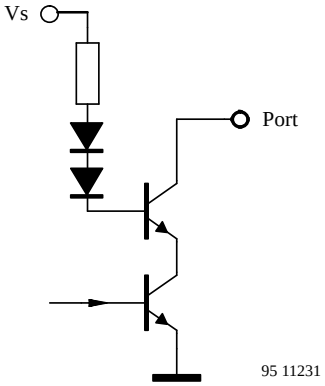


Figure 10. Ports

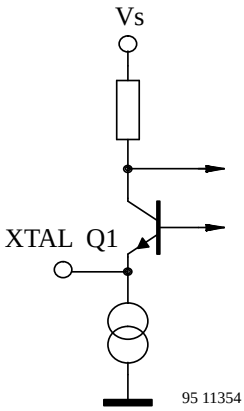


Figure 8. Reference oscillator

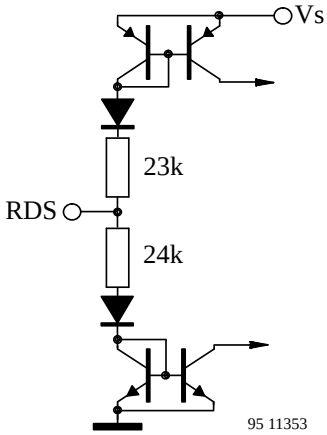


Figure 11. Reference divider select input

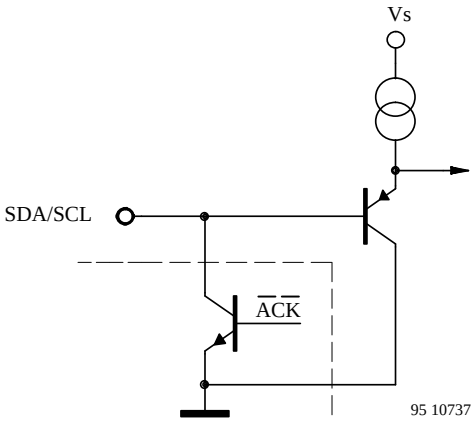


Figure 9. SCL and SDA input

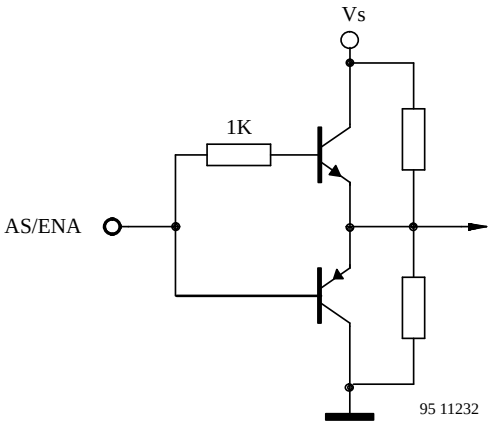


Figure 12. Address select/ Enable input

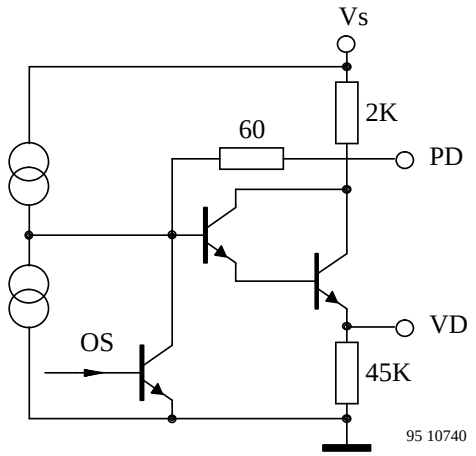


Figure 13. Loop amplifier

Typical Prescaler Input Sensitivity

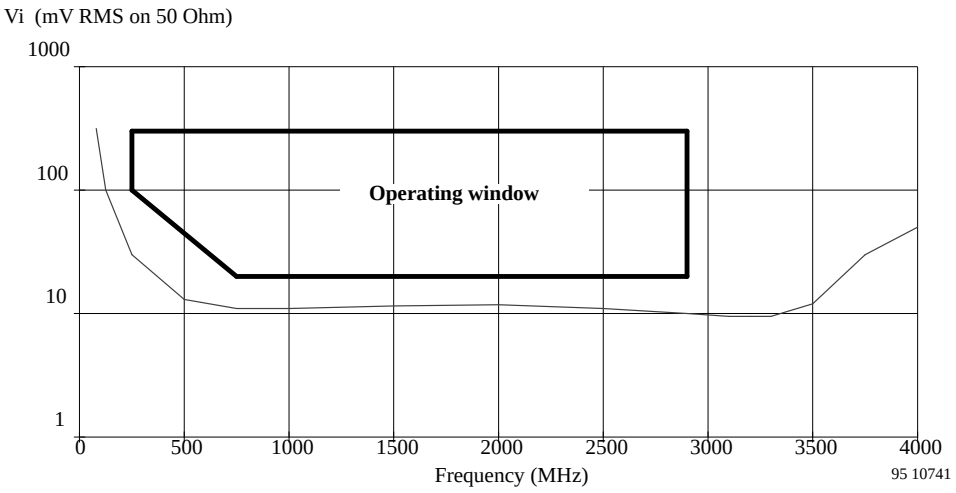


Figure 14.

Typical Input Impedance

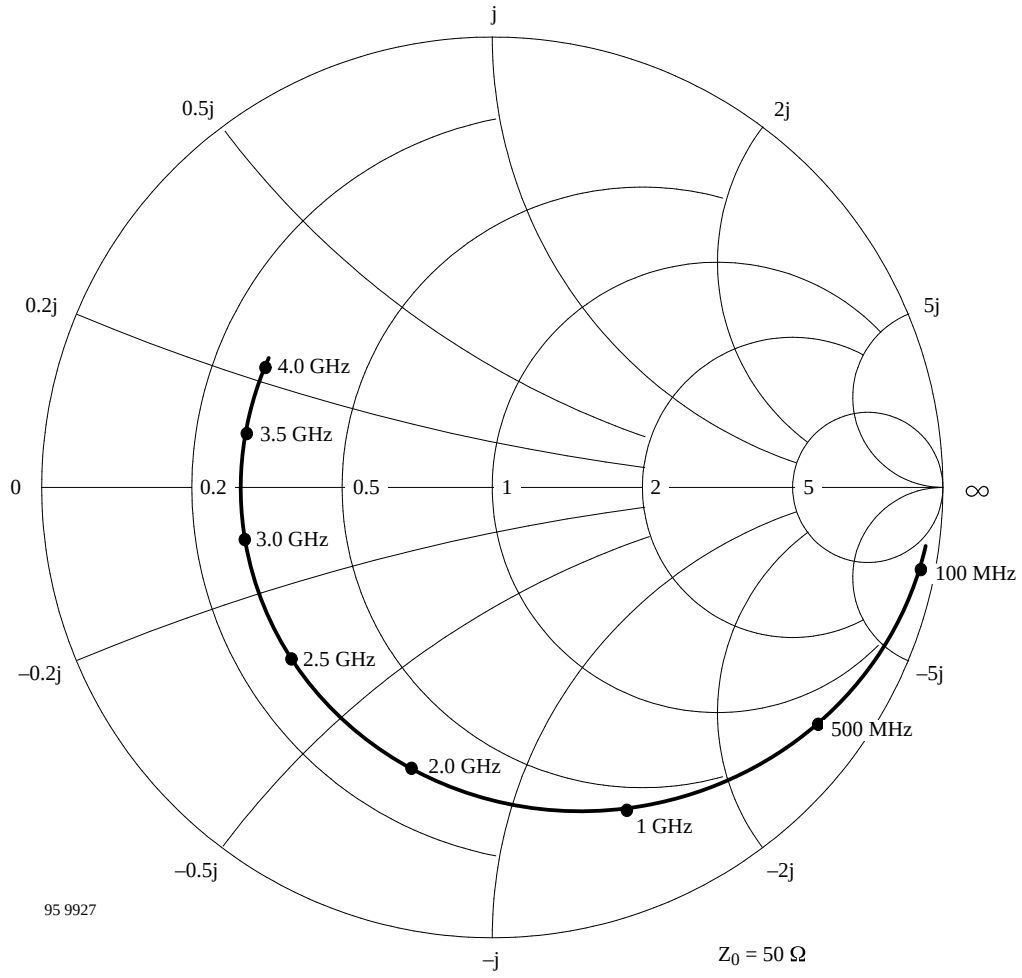


Figure 15.

Application Circuit

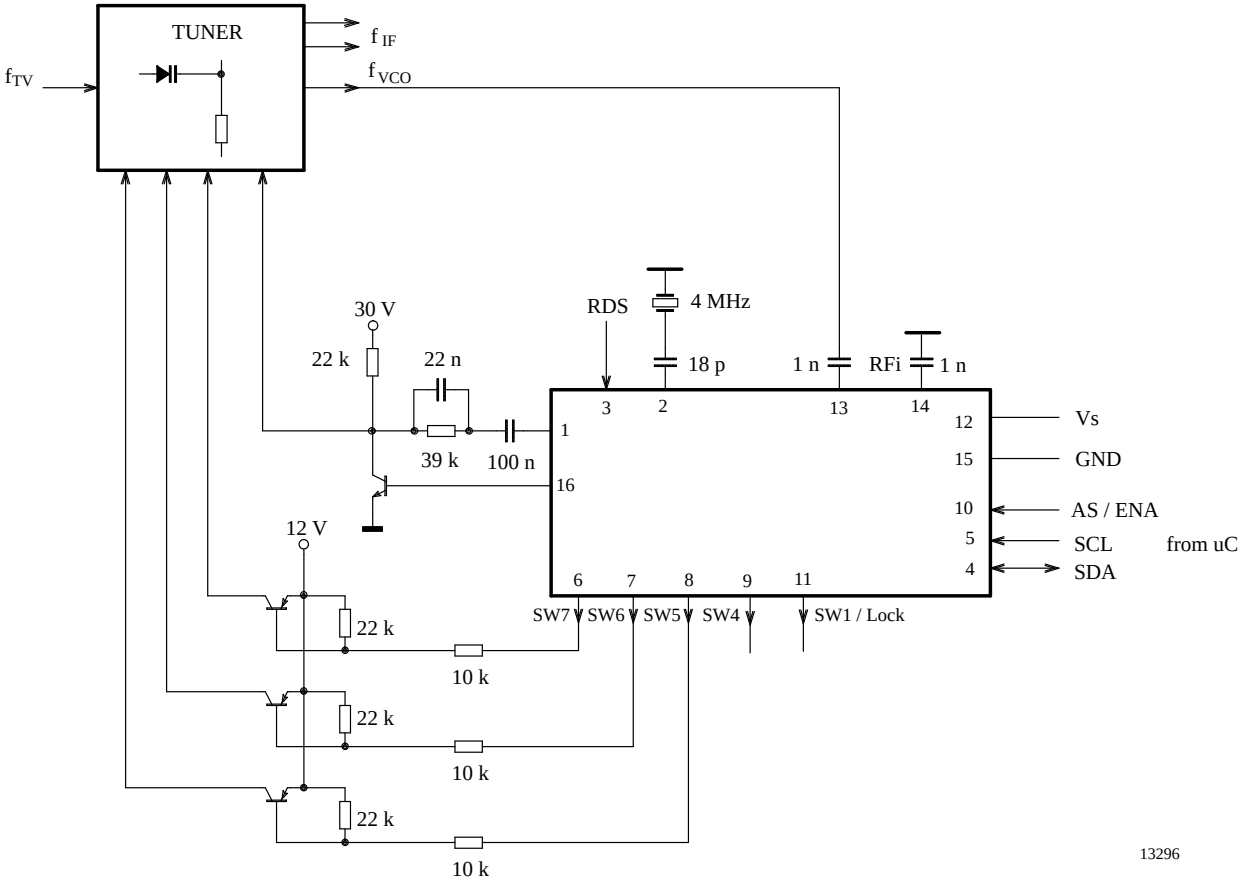
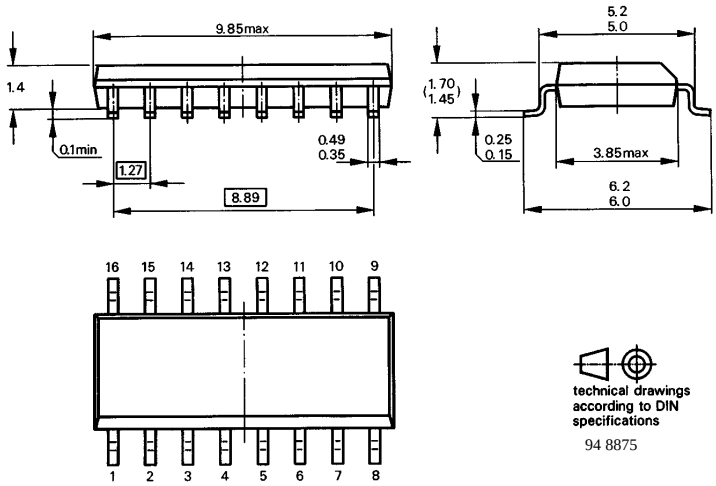


Figure 16.

Package Dimensions

Small outline plastic package, 16 pin-SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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